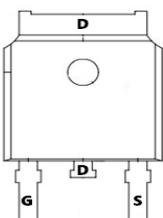
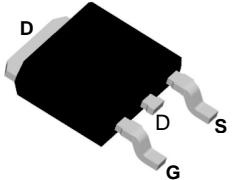
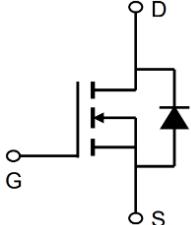


TM55N10D
N-Channel Enhancement Mosfet

General Description <ul style="list-style-type: none"> • Low R_{DS(ON)} • RoHS and Halogen-Free Compliant Applications <ul style="list-style-type: none"> • Load switch • PWM 	General Features <p> $V_{DS} = 100V$ $I_D = 55A$ $R_{DS(ON)} = 15 m\Omega$(typ.) @ $V_{GS} = 10V$ 100% UIS Tested 100% R_g Tested </p> 
---	---

 Marking:55N10	D:TO-252-3L 	
--	---	---

Absolute Maximum Ratings ($T_A = 25^\circ C$ Unless Otherwise Noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	100	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	55	A
Drain Current-Continuous($T_C=100^\circ C$)	$I_D (100^\circ C)$	28	A
Pulsed Drain Current	I_{DM}	160	A
Maximum Power Dissipation	P_D	140	W
Derating factor	-	0.93	W/ $^\circ C$
Single pulse avalanche energy ^(Note 5)	E_{AS}	350	mJ
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 175	$^\circ C$

Thermal Characteristic

Thermal Resistance,Junction-to-Case ^(Note 2)	$R_{\theta JC}$	1.07	$^\circ C/W$
---	-----------------	------	--------------

Electrical Characteristics ($T_c=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{\text{GS}}=0\text{V}, I_{\text{D}}=250\mu\text{A}$	100	-	-	V
Zero Gate Voltage Drain Current	$I_{\text{DS}}^{\text{SS}}$	$V_{\text{DS}}=100\text{V}, V_{\text{GS}}=0\text{V}$	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	$V_{\text{GS}}=\pm20\text{V}, V_{\text{DS}}=0\text{V}$	-	-	±100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	$V_{\text{GS}(\text{th})}$	$V_{\text{DS}}=V_{\text{GS}}, I_{\text{D}}=250\mu\text{A}$	0.9	1.3	1.6	V
Drain-Source On-State Resistance	$R_{\text{DS}(\text{ON})}$	$V_{\text{GS}}=10\text{V}, I_{\text{D}}=20\text{A}$	-	15	18	$\text{m}\Omega$
		$V_{\text{GS}}=4.5\text{V}, I_{\text{D}}=20\text{A}$	-	18	20	
Forward Transconductance	g_{FS}	$V_{\text{DS}}=5\text{V}, I_{\text{D}}=20\text{A}$	32	-	-	S
Dynamic Characteristics (Note4)						
Input Capacitance	C_{iss}	$V_{\text{DS}}=50\text{V}, V_{\text{GS}}=0\text{V}, F=1.0\text{MHz}$	-	3700	-	PF
Output Capacitance	C_{oss}		-	176	-	PF
Reverse Transfer Capacitance	C_{rss}		-	148	-	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	$t_{\text{d}(\text{on})}$	$V_{\text{DD}}=30\text{V}, R_{\text{L}}=1.5\Omega, R_{\text{G}}=2.5\Omega, V_{\text{GS}}=10\text{V}$	-	15	-	nS
Turn-on Rise Time	t_{r}		-	11	-	nS
Turn-Off Delay Time	$t_{\text{d}(\text{off})}$		-	52	-	nS
Turn-Off Fall Time	t_{f}		-	13	-	nS
Total Gate Charge	Q_{g}	$I_{\text{D}}=20\text{A}, V_{\text{DD}}=50\text{V}, V_{\text{GS}}=10\text{V}$	-	119	-	nC
Gate-Source Charge	Q_{gs}		-	11.4	-	nC
Gate-Drain Charge	Q_{gd}		-	22.9	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V_{SD}	$V_{\text{GS}}=0\text{V}, I_{\text{S}}=20\text{A}$	-	0.85	1.2	V
Diode Forward Current (Note 2)	I_{S}		-	-	55	A
Reverse Recovery Time	t_{rr}	$T_{\text{J}} = 25^\circ\text{C}, I_{\text{F}} = 20\text{A}$ $di/dt = 100\text{A}/\mu\text{s}$ (Note3)	-	33		nS
Reverse Recovery Charge	Q_{rr}		-	54		nC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production
5. EAS condition: $T_j=25^\circ\text{C}, V_{\text{DD}}=50\text{V}, V_{\text{G}}=10\text{V}, L=0.5\text{mH}, R_g=25\Omega$

Typical Electrical and Thermal Characteristics (Curves)

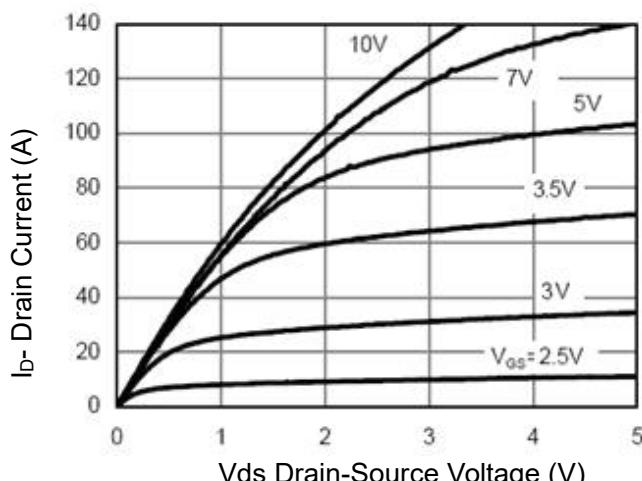


Figure 1 Output Characteristics

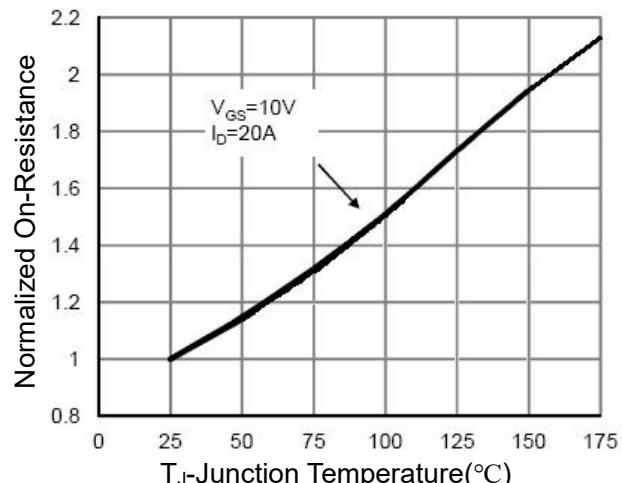


Figure 4 Rdson-JunctionTemperature

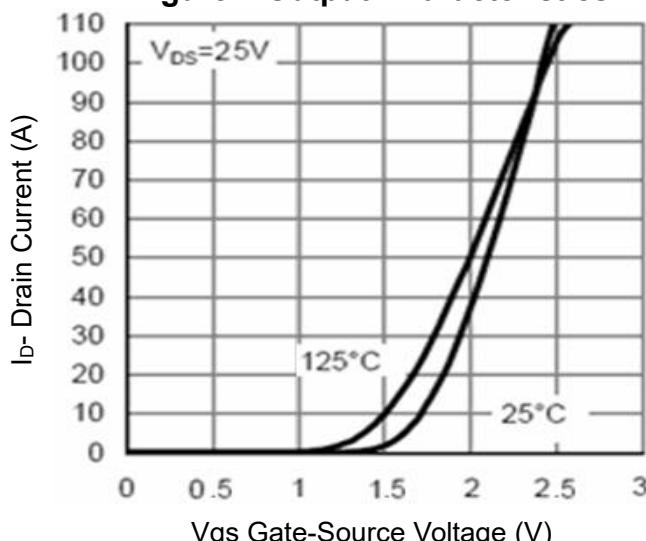


Figure 2 Transfer Characteristics

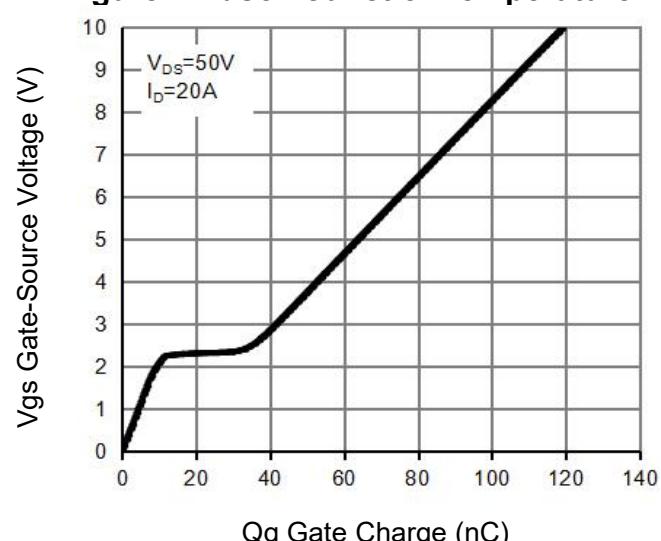


Figure 5 Gate Charge

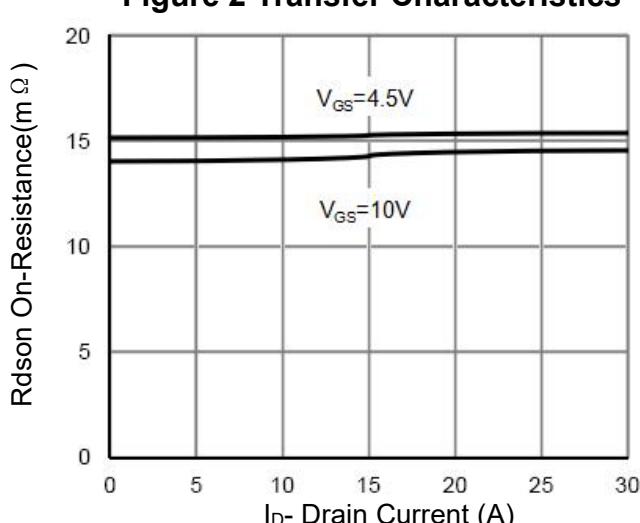


Figure 3 Rdson- Drain Current

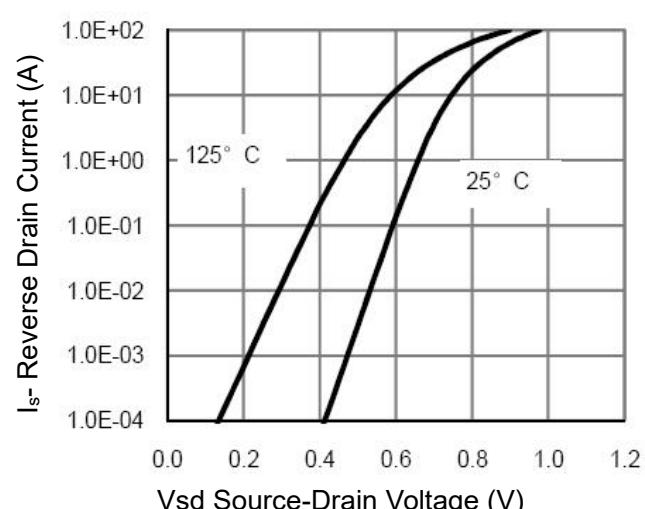


Figure 6 Source- Drain Diode Forward

TM55N10D

N-Channel Enhancement Mosfet

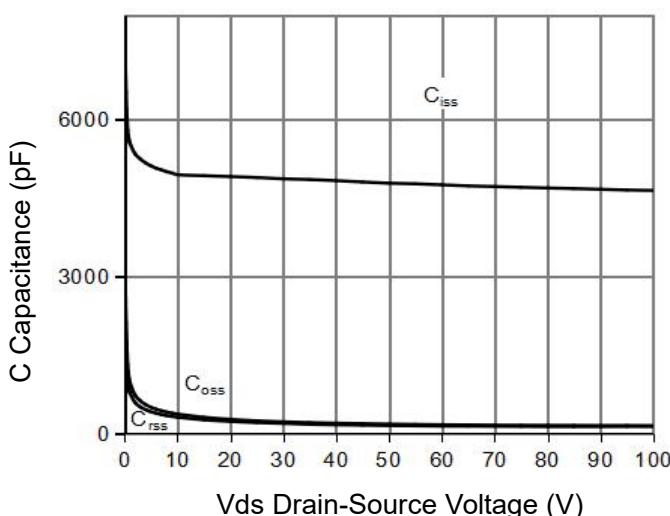


Figure 7 Capacitance vs Vds

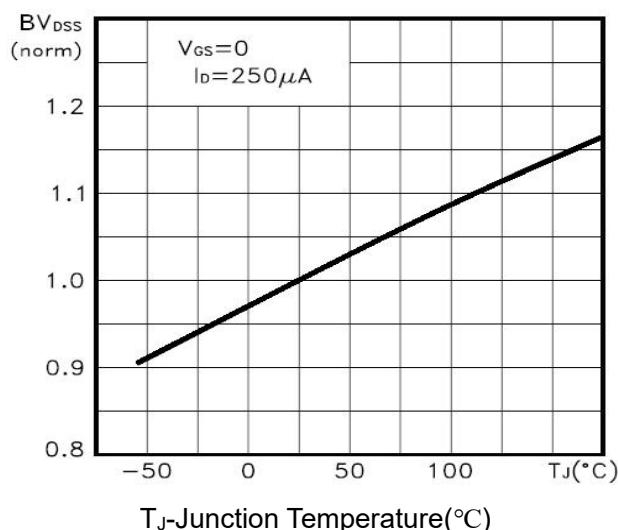


Figure 9 BV_{dss} vs Junction Temperature

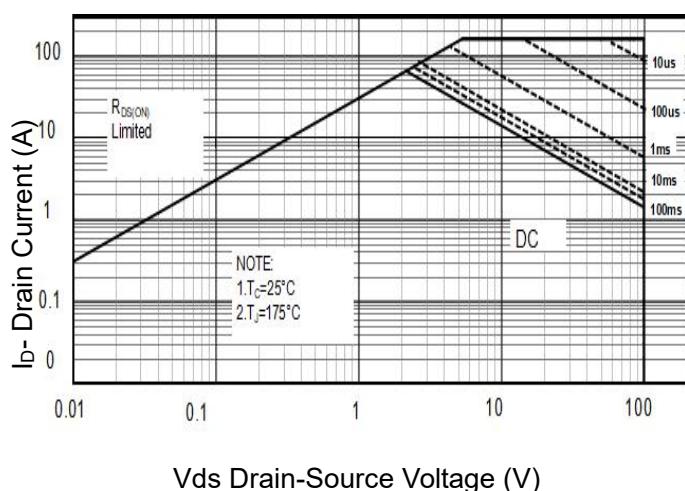


Figure 8 Safe Operation Area

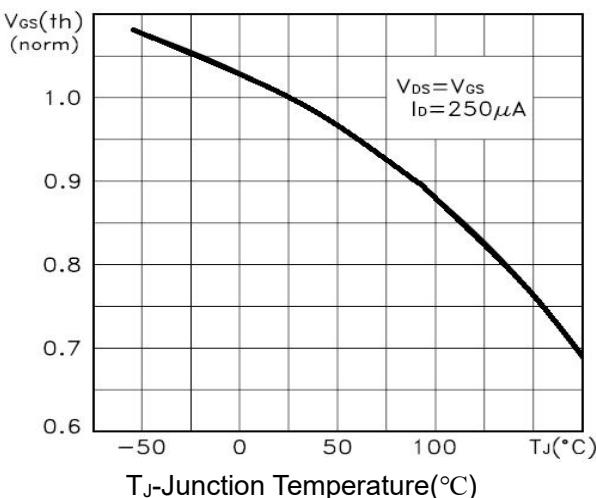


Figure 10 $V_{GS(th)}$ vs Junction Temperature

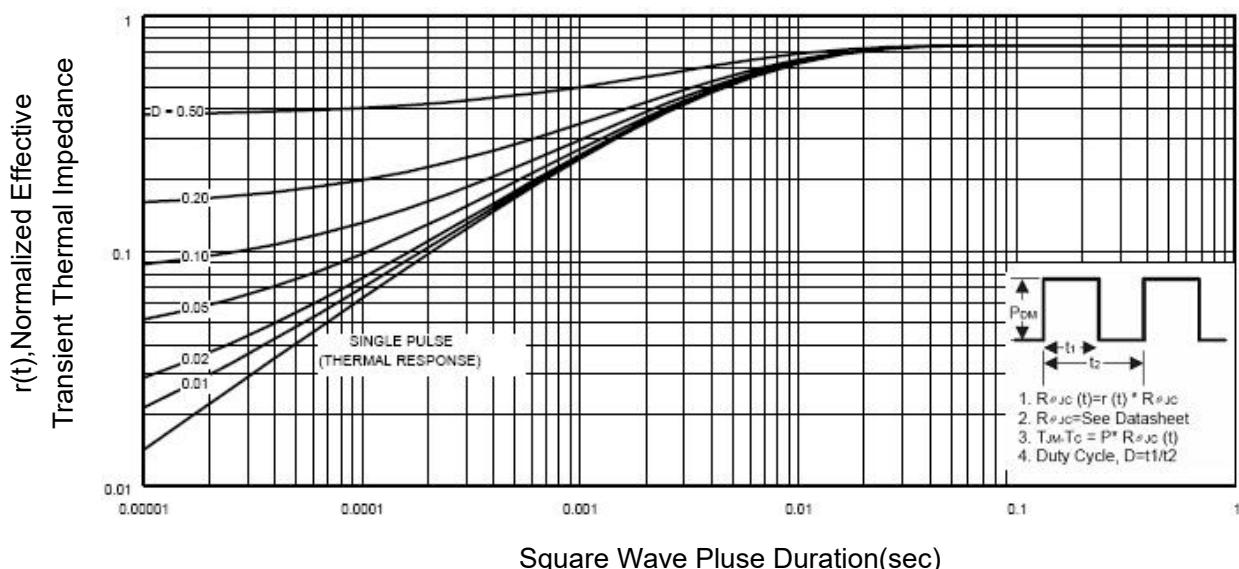
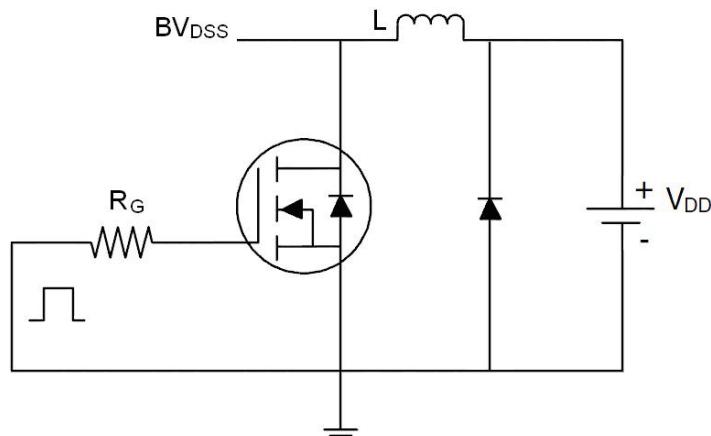


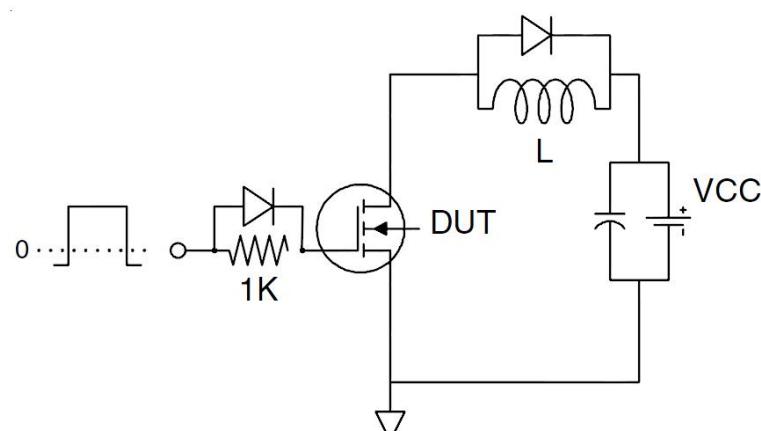
Figure 11 Normalized Maximum Transient Thermal Impedance

Test Circuit

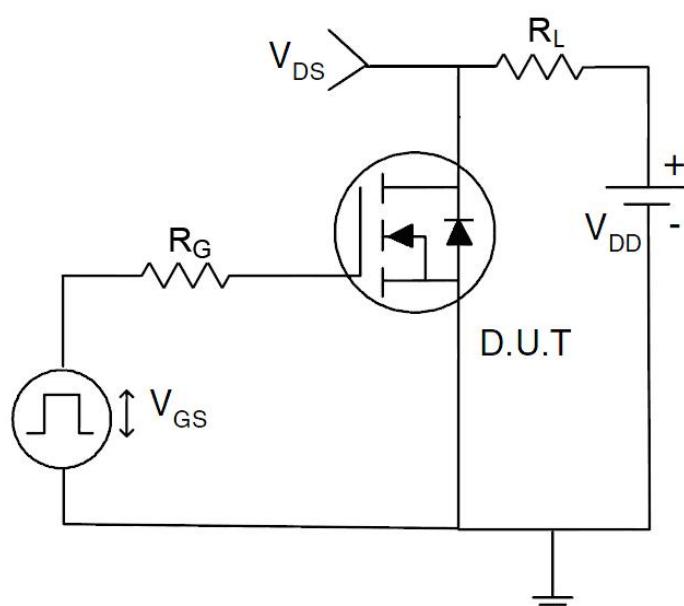
1) E_{AS} test Circuit



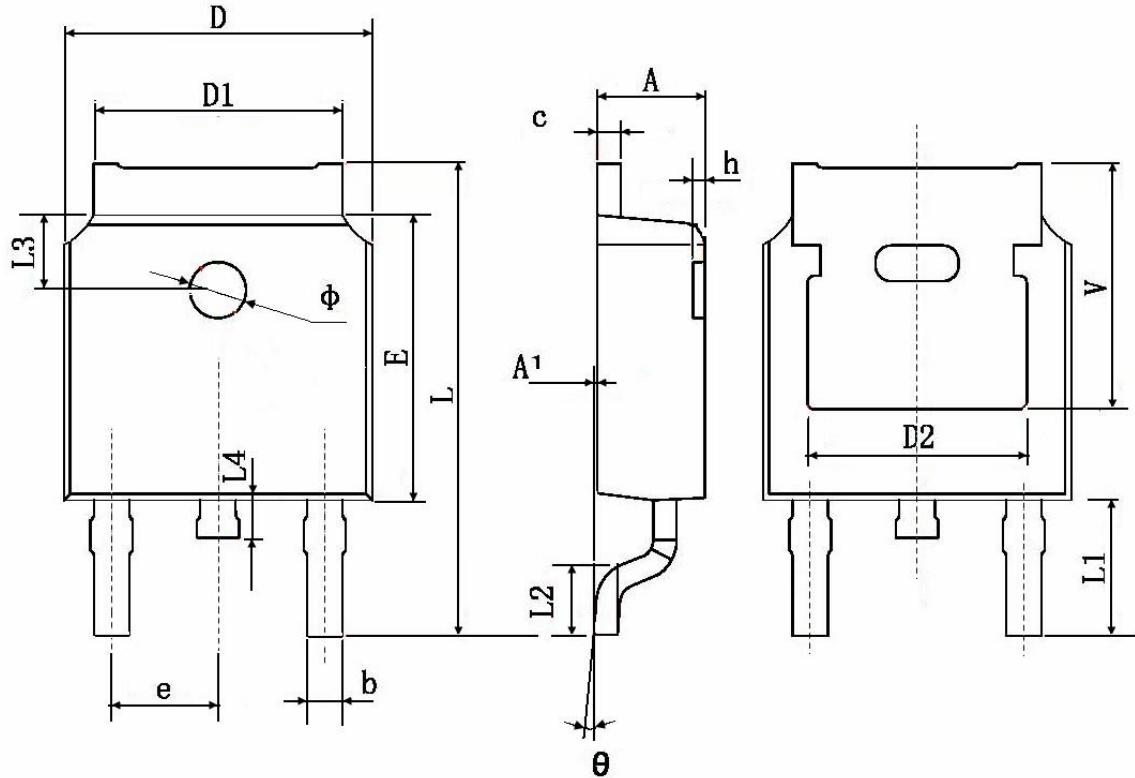
2) Gate charge test Circuit



3) Switch Time Test Circuit



Package Information: TO-252-3L



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	2.200	2.400	0.087	0.094
A1	0.000	0.127	0.000	0.005
b	0.660	0.860	0.026	0.034
c	0.460	0.580	0.018	0.023
D	6.500	6.700	0.256	0.264
D1	5.100	5.460	0.201	0.215
D2	4.830 TYP.		0.190 TYP.	
E	6.000	6.200	0.236	0.244
e	2.186	2.386	0.086	0.094
L	9.800	10.400	0.386	0.409
L1	2.900 TYP.		0.114 TYP.	
L2	1.400	1.700	0.055	0.067
L3	1.600 TYP.		0.063 TYP.	
L4	0.600	1.000	0.024	0.039
Φ	1.100	1.300	0.043	0.051
θ	0°	8°	0°	8°
h	0.000	0.300	0.000	0.012
V	5.350 TYP.		0.211 TYP.	